Course Title:	**Hardware Description Language Verilog**
Institute/Division:	Department of Automation and Computer Engineering Faculty of Electrical and Computer Engineering
Course code:	**E-HLV**
Erasmus subject code:	0611 Computer use
Number of contact hours:	45
Course duration:	1 semester (Spring/Summer)
ECTS credits:	6
Course description:	The course includes lectures and computer laboratory exercises. The aim of the course is to familiarize the student with the basic syntax and basic language constructs of Verilog and computer simulation tools. • Introduction to Verilog. Modeling at the behavioral, structural, register transfer (RTL) and logical equations levels of digital systems in Verilog. Sequential and concurrent operations. • Basic functional modules and syntax elements of the Verilog language. • Synthesis and simulation of combinational circuits. Adders, encoders, decoders, multiplexers. • Synthesis and simulation of sequential circuits. Counters, registers. • Synthesis and types of memory circuits in programable circuits. • Designing Moore and Mealy Digital Automata in Verilog. • Optimal design of state machines. • Behavioral simulations of designed structures in the ALDEC Active Verilog environment • The issue of optimizing hardware resources and system speed. • New Trends and Languages in Programmable Logic Technology. Intended software: Active VHDL / (Verilog) design and simulation tool from ALDEC company At-home practice: possible installation on a private computer of the Active VHDL/(Verilog).
Course type:	Lectures (15h), Laboratory (30h)
Literature:	Palnitkar Samir, *Verilog HDL. A guide to Digital Design and Synthesis.* SunSoft Press 1996. Bhasker J., *Verilog HDL Synthesis. A practical Primer.* Star Galaxy Publishing 1998. Blandford D. K., *Verilog tutorial*, University of Evansville 2004. Online tutorial: https://www.asic-world.com/verilog/veritut.html

Assessment method:	Final project, laboratory exercises
Prerequisites:	-
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