Course Title:	**Programmable Digital Systems**
Institute/Division:	Department of Automation and Computer Engineering Faculty of Electrical and Computer Engineering
Course code:	**E-PDS**
Erasmus subject code:	0714 Electronics and automation
Number of contact hours:	45
Course duration:	1 semester (Fall/Winter)
ECTS credits:	6
Course description:	The course includes lectures , computer laboratory exercises, and individual projects. The aim of the course is to gather knowledge about modern FPGA architectures, HDL languages and FPGA programmable logic technology. Laboratory and practical project courses are aimed at supporting students' design skills. • Architectures of digital FPGA systems dedicated to applications in computer systems. • Overview of architectures of selected FFGAs and their applications. • Xilinx tools for designing, programming and verifying FPGA systems (ISE/Vivado/Vitis.) • MicroBlaze / RISC-V Processor Cores implemented in FPGA. • Specialized IP architectures for DSP computations. Aspects of function decomposition between microprocessor and programmable logic systems. • Generating DSP modules using Matlab HDL coder. • Communication between a digital system and a microprocessor. Peripheral system interfaces – AXI, SPI, I2C. • Communication between the microcontroller and the A/D or C/A converter. • Synthesis and implementation of C/C++ language functions using Xilinx Vitis tools. • New soft-core processor cores implemented in FPGA / Xilinx platform Verslal ACAP for Artificial Inteligence (AI). Intended software: Xilinx Vitis/Vivado, Xilinx ISE 14.7, Matlab HDL coder At-home practice: possible installation on a private computer of the Xilinx ISE 14.7, Matlab HDL coder.
Course type:	Lectures (14h), Laboratory (16h), Project (15h)
Literature:	Richard S. Sandige, *Digital and computer design in VHDL*, New York, 2012, McGraw-Hill. Enoch O. Hwang, *Microprocessor Design Principles and Practices With VHDL*, 2004, Brooks/Cole *IEEE Standard Verilog Hardware Description Language*. IEEE Computer Society. New York 2001.

	Douglas J. Smith, *HDL Chip Design* 1997. Bhasker J., *Verilog HDL Synthesis. A practical Primer*. Star Galaxy Publishing 1998. Blandford D. K., *Verilog tutorial,* University of Evansville 2004. Online tutorial: https://www.asic-world.com/verilog/veritut.html Xilinx, *MicroBlaze Processor Reference Guide*, San Jose, CA, 2018, Xilinx UG984. Xilinx, *Versal ACAP Technical Reference Manual*, San Jose, CA, 2024, Xilinx AM011
Assessment method:	The final project, laboratory exercises
Prerequisites:	-
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