Course Title:	**Hardware Description Language VHDL**
Institute/Division:	Department of Automation and Computer Engineering Faculty of Electrical and Computer Engineering
Course code:	**E-VHDL**
Erasmus subject code:	0611 Computer use
Number of contact hours:	45
Course duration:	1 semester (Spring/Summer)
ECTS credits:	6
Course description:	The course includes lectures and computer laboratory exercises. The aim of the course is to familiarize the student with the basic syntax and basic language constructs of VHDL (Very High Description Language) and computer simulation tools. • Introduction to VHDL. Modeling at the behavioral, structural, register transfer (RTL) and logical equations levels of digital systems in VHDL. Sequential and concurrent operations. • Basic functional modules and syntax elements of the VHDL language. • Synthesis and simulation of combinational circuits. Adders, encoders, decoders, multiplexers. • Synthesis and simulation of sequential circuits. Counters, registers. • Synthesis and types of memory circuits in programable circuits. • Designing Moore and Mealy Digital Automata in VHDL. • Optimal design of state machines. • Behavioral simulations of designed structures in the ALDEC Active VHDL environment • The issue of optimizing hardware resources and system speed. • New Trends and Languages in Programmable Logic Technology. Intended software: Active VHDL design and simulation tool from ALDEC company At-home practice: possible installation on a private computer of the Active VHDL (student free version of license).
Course type:	Lectures (15h), Laboratory (30h)
Literature:	Douglas L. Perry, *VHDL Programming by examples*, San Francisco, 2002, McGraw-Hill. Peter J. Ashenden, *The VHDL Cook book*, Australia, 1990, University of Adelaide South Australia. Richard S. Sandige, *Digital and computer design in VHDL*, New York, 2012, McGraw-Hill.
Assessment method:	Final project, laboratory exercises
Prerequisites:	-
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